REMARKS

The following remarks are being submitted as a full and complete response to the Office Action dated July 14, 2008 the telephone interview with the Examiner conducted on September 4, 2008, the Advisory Action dated December 5, 2008, and the Notice of Appeal filed on December 12, 2008. Applicants thank the Examiner for taking the time to conduct the telephone interview. In view of the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1, 3-10, 12-24 and 29-33 are under consideration in this application. Claims 2 and 11 are being cancelled without prejudice or disclaimer. Claim 1 is being amended to correct formal errors and to more particularly point out and distinctly claim the subject invention. Claims 32-33 are being added. All the amendments to the claims are supported by the specification. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Interview Summary

Applicants, through their representative, Jennifer Teng, compared Fig. 2 of the present invention with Fig. 2 of Stewart, and explained to the Examiner that Stewart only supplies a constant voltage to a power supply line D2 connected to a source/drain of the OLED 210 in the illuminated period, but not to a signal line D1 connected to the gate of the OLED 210 in the illuminated period, as in the present invention. The Examiner indicated that he will take the explanation into consideration when he receives a formal response, since the case is under final rejection.

Prior Art Rejections

Under 35 U.S.C. §103(a), the Examiner rejected: (1) Claims 1-4, 6-7, 9, 12-15, 17-18, 20, 23-24 and 29-31 as being unpatentable over US Publication No. 2003/0067424 to Akimoto et al. in view of newly cited US Patent No. 5,952,789 to Stewart et al.; (2) Claims 5, 8, 16 and 19 as being unpatentable over Akimoto '424 in view of Stewart '789, and further in view of US Patent No. 5,250,931 to Misawa et al.; (3) Claims 10 and 21 as being unpatentable over Akimoto '424 in view of Stewart '789, and further in view of US Patent No. 6,670,936 to Akimoto et al.; and (4) Claims 11 and 22 as being unpatentable over

Akimoto '424 in view of Stewart '789, and further in view of US Patent No. 6,812,912 to Miyajima et al. These rejections have been carefully considered, but are most respectfully traversed.

The image display device of the present invention (for example, the First Embodiment depicted in Figs. 1-5), as now recited in claim 1, comprises: a display part 20 configured by a plurality of pixels 10 each having an electro-luminescent element 1 driven to illuminate according to a display signal voltage Vs, and said pixels being disposed in a matrix (Fig. 1); a signal line 8 used to write said display signal voltage Vs in said pixels 10 and located in a direction of a column of the matrix (during a "writing period", 1st half of a frame in Fig. 3 with the timing details shown in Fig. 4); a pixel selector 15 for selecting a pixel from said plurality of pixels so as to write said display signal voltage Vs therein through said signal line 8; a display signal voltage generator 16 for generating said display signal voltage Vs; an illuminating state controller for controlling a selection of an illuminating state or a non-illuminating state for each of said plurality of pixels at a time; and a constant voltage supply for supplying a constant voltage Vil to each of said plurality of pixels through said signal line 8 when said illuminating state is selected for said selected pixel. One end of said electro-luminescent element 1 provided in each said pixel 10 is connected to a common power supply while the other end of said electro-luminescent element 1 is selectively connected to a first source/drain electrode of an electro-luminescent element driving transistor 2 through a first switch 7, said transistor 2 has a threshold voltage Vth, a second source/drain electrode of said electro-luminescent element driving transistor 2 is connected to a power supply line 9 applied with a prescribed voltage (from a power input line 13 in Fig. 1), and the gate of said electro-luminescent element driving transistor 2 is connected to the signal line 8 through a capacitance 4 and selectively connected to the first source/drain electrode of said electro-luminescent element driving transistor 2 through a second switch 6 (claim 2; Fig. 2). When said illuminating state is selected (during a "illuminating period", 2nd half of the frame in Fig. 3), the first switch 7 is fixed as ON, the second switch 6 is fixed as OFF, and the constant voltage Vil lower than display signal voltage Vs is applied to the signal line 8 (Fig. 1; "*the signal line switch 17 switches the signal line 8 between the signal voltage generation circuit 16 and the constant voltage input line 14*" p. 10, lines 1-4) such that a voltage that is lower than said prescribed voltage (e.g., by (Vs-Vil+ |Vth|); claim 29) appears at the gate of said transistor 2 (Fig. 3; p. 13, lines 19-25; p. 14, lines 5-11).

In particular, a gate wiring 21 forming the gate of said transistor 2 extends in the direction of the column of the matrix so as to overlap with the signal line 8, and an overlap

between the signal line 8 and the sate wiring 21 forms the capacitance 4 (claim 2; Fig. 5; *"The gate wiring 21 is laid out so as to be overlapped with part of the signal line 8, thereby the part of the signal line 8 comes to be used as the storage capacitor 4 as is."* p. 15, last para.).

This characteristic makes it possible to expand the area of the transparent electrode 25 and the organic EL, and to reduce the driving voltage required for the organic EL to illuminate.

As admitted by the Examiner, neither Akimoto nor Stewart disclose the connection capacitor provided on the signal line in layers as recited in claim 11. Maejima's element 30 (Fig. 14) provided on a signal line in layers was relied upon by the Examiner to cover the teaching (p. 11, 2nd to last para. of the outstanding Office Action). However, the alleged capacitor is merely a first electrode 30 of a storage capacitor (col. 17, lines 42-43), rather than the capacitor itself. This is because that a conductive shielding layer 20e (to which a prescribed voltage is applied) is formed between the layers in the superimposed region of the first electrode 30 and the data line 22 in order to prevent coupling (col. 17, lines 38-55). As such, Maejima fails to teach any capacitor provided on the signal line. Therefore, Maejima does not disclose that "a gate wiring 21 forming the gate of said transistor extends in the direction of the column of the matrix so as to overlap with the signal line 8, and an overlap between the signal line 8 and the sate wiring 21 forms the capacitance 4" as in the present invention.

The image display device of the present invention (for example, the Second Embodiment depicted in Fig. 6; pp. 20-21), as now recited in claim 32, comprises the major elements of claim 1, and additionally recites that each of the electro-luminescent element driving transistor 2, the first switch 7, the second switch 6 and the capacitance 4 is formed with a **p-type** transistor (claims 4-5, 15-16), a gate of the p-type transistor forming the capacitance 4 is connected to the gate of the electro-luminescent element driving transistor 2, source and drain electrodes of the p-type transistor forming the capacitance 4 are connected to the signal line 8, and **the signal voltage Vs is set so as to become lower than a *difference* of the prescribed voltage of the power supply line 9 minus the threshold voltage Vth** (*"the signal voltage applied to the signal line 8 is set so as to become lower than the resetting time voltage of the driving TFT (the voltage of the power supply line 9 - |Vth|)."* p. 20, last para.).

Consequently, a channel is always formed in the p-type polycrystalline silicon TFT used as the storage capacitor 34 so as to stabilize the gate capacitor.

The image display device of the present invention (for example, the Fourth Embodiment depicted in Fig. 12; pp. 29-31), as now recited in claim 33, comprises the major elements of claim 1, and additionally recites that each of the electro-luminescent element driving transistor, the first switch, the second switch and the capacitance is formed with an **n-type** transistor (claims 7-8 and 18-19), a gate of the n-type transistor forming the capacitance is connected to the gate of the electro-luminescent element driving transistor, source and drain electrodes of the n-type transistor forming the capacitance are connected to the signal line, and **the signal voltage Vs is set so as to become lower than a *sum* of the prescribed voltage of the power supply line 9 plus the threshold voltage Vth** ("*the signal voltage applied to the signal line 8 is set so as to become lower than the resetting time voltage of the driving TFT 62 (the voltage of the power supply line 9 +|Vth|.)*." p. 29, last para.).

Consequently, a channel is always formed at the n-type amorphous silicon TFT used as the storage capacitor 64, thereby the gate capacitor is usable as a stable capacitor.

As admitted by the Examiner, neither Akimoto nor Stewart disclose the connection capacitor is p-type or n-type transistor as recited in claims 5, 8, 16 & 19. Misawa's pixel capacitor 305 (Figs. 15a-b) was relied upon by the Examiner to cover the teachings (p. 9 of the outstanding Office Action). However, Misawa does not set the signal voltage Vs to be lower than "a *difference* of the prescribed voltage of the power supply line minus the threshold voltage Vth" or "a *sum* of the prescribed voltage of the power supply line plus the threshold voltage Vth" as in the present invention.

Applicants contend that neither Akimoto, Stewart, Maejima, Misawa, nor their combinations teach or suggest each and every feature of the present invention as disclosed in independent claims 1 and 32-33. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

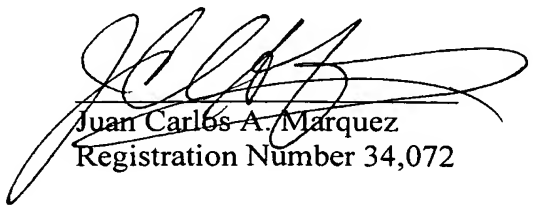
Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance

of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

Respectfully submitted,



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